DUAL POWER SENSING SCHEME FOR A MEMORY DEVICE

ABSTRACT

Sensing operations involving a first array of bit line sense amplifiers (BLSAs) may be powered by an upper reference voltage and a first intermediate voltage and the first array may be precharged to a voltage level therebetween. Sensing operations involving a second array of BLSAs may be powered by a second intermediate voltage (greater than the first intermediate voltage) and a lower reference voltage and the second array may be precharged to a voltage level therebetween. After precharge, charge may be transferred from a second power line of the first array to a first power line of the second array. Subsequently, the second power line of the first array may be coupled to a power supply node at the first intermediate voltage level and the first power line of the second array may be coupled to a power supply node at the second intermediate voltage level.